SCAS090 - DECEMBER 1989 - REVISED APRIL 1993

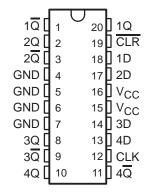
- Applications Include: Buffer/Storage Registers, Shift Registers, Pattern Generators
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V<sub>CC</sub> and GND Configurations Minimize High-Speed Switching Noise
- EPIC<sup>™</sup> (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

### description

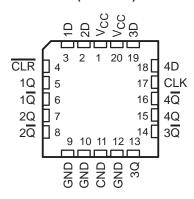
These positive-edge-triggered flipflops implement D-type flip-flop logic with a direct clear input. Information at the D inputs that meets the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

The 54AC11175 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The 74AC11175 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

#### 54AC11175 . . . J PACKAGE 74AC11175 . . . DW or N PACKAGE (TOP VIEW)



## 54AC11014 . . . FK PACKAGE (TOP VIEW)



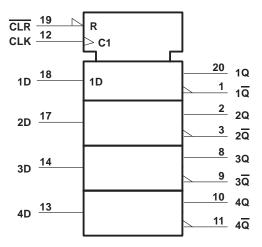
FUNCTION TABLE (each flip-flop)

ı	NPUTS	OUTI	PUTS	
CLR	CLK	D	Q	Q
L	Х	Χ	L	Н
Н	$\uparrow$	Н	Н	L
Н	$\uparrow$	L	L	Н
Н	L	Χ	Q <sub>0</sub>	$\overline{Q}_0$

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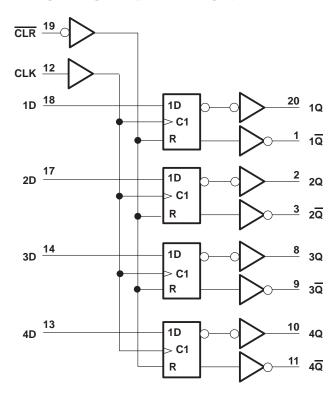
### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the DW, J and N packages.

### logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>	−0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	±20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±50 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through V <sub>CC</sub> or GND	±200 mA
Storage temperature range	

<sup>‡</sup>Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.



### recommended operating conditions

			54	54AC11175		74AC11175			LINUT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		3	5	5.5	3	5	5.5	V
		V <sub>CC</sub> = 3 V	2.1			2.1			
$V_{IH}$	High-level input voltage	V <sub>CC</sub> = 4.5 V	3.15			3.15			V
		V <sub>CC</sub> = 5.5 V	3.85		4	3.85			
		VCC = 3 V		Ś	<b>4</b> 0.9			0.9	
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 4.5 V		2	1.35			1.35	V
		V <sub>CC</sub> = 5.5 V		70	1.65			1.65	
		V <sub>CC</sub> = 3 V		5	-4			-4	
loh	High-level output current	VCC = 4.5 V	Ĉ	37	-24			-24	mA
		V <sub>CC</sub> = 5.5 V	2		-24			-24	
		V <sub>CC</sub> = 3 V			12			12	
l <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 4.5 V			24			24	mA
		V <sub>CC</sub> = 5.5 V			24			24	
٧ <sub>I</sub>	Input voltage		0	•	Vcc	0		Vcc	V
٧o	Output voltage		0		Vcc	0		Vcc	V
Δt/Δν	Input transition rise or fall rate		0		10	0		10	ns/V
TA	Operating free-air temperature		-55		125	-40		85	°C

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS	V	T	λ = 25°C	;	54AC1	1175	74AC1	1175	HAUT
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
		3 V	2.9			2.9		2.9		
	ΙΟΗ = - 50 μΑ	4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
Vou	$I_{OH} = -4 \text{ mA}$	3 V	2.58			2.4	Ŋ	2.48		V
VOH	laura 24 mA	4.5 V	3.94			3.7	VIE	3.8		V
	I <sub>OH</sub> = - 24 mA	5.5 V	4.94			4.7	A	4.8		
	$I_{OH} = -50 \text{ mA}^{\dagger}$	5.5 V				3.85				
	$I_{OH} = -75 \text{ mA}^{\dagger}$	5.5V				20		3.85		
		3 V			0.1	<sup>j</sup> A <sub>O</sub>	0.1		0.1	
	I <sub>OL</sub> = 50 μA	4.5 V			0.1	/	0.1		0.1	
		5.5 V			0.1		0.1		0.1	
V	I <sub>OL</sub> = 12 mA	3 V			0.36		0.5		0.44	V
VOL	lo 24 mA	4.5 V			0.36		0.5		0.44	V
	I <sub>OL</sub> = 24 mA	5.5 V			0.36		0.5		0.44	
	I <sub>OL</sub> = 50 mA	5.5 V					1.65			
	$I_{OL} = 75 \text{ mA}^{\dagger}$	5.5 V							1.65	
ΙĮ	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		160		80	μΑ
C <sub>i</sub>	$V_I = V_{CC}$ or GND	5 V		4						pF

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.



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## timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

			T <sub>A</sub> =	T <sub>A</sub> = 25°C		T <sub>A</sub> = 25°C		T <sub>A</sub> = 25°C 54AC11175		74AC11175		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	ONT			
fclock	Clock frequency		0	90	0	90	0	90	MHz			
A Dulas duration	Pulse duration	CLR low	5.5		5.5	10,1	5.5					
t <sub>W</sub>	Fulse duration	CLK high or low	5.5		5.5	IL.	5.5		ns			
	Octor force to force OLIVA	Data	8		8		8					
t <sub>Su</sub> Setup tir	Setup time before CLK↑	CLR inactive			8		8		ns			
t <sub>h</sub>	Hold time, data after CLK↑		0.5		0.5		0.5		ns			

# timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

			T <sub>A</sub> =	T <sub>A</sub> = 25°C		T <sub>A</sub> = 25°C		1175	74AC11175		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	ONIT		
fclock	Clock frequency		0	125	0	125	0	125	MHz		
t Dulas d	Pulse duration	CLR low	4		4	(C)	4		20		
t <sub>W</sub>	Pulse duration	CLK high or low	4		45		4		ns		
	Catur time hafara CLIVA	Data	5.5		5.5		5.5		no		
t <sub>su</sub> Setup	Setup time before CLK↑	CLR inactive			5.5		5.5		ns		
t <sub>h</sub>	Hold time, data after CLK↑		0.5		0.5		0.5		ns		

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

DADAMETED	PARAMETER FROM TO		T,	չ = 25°C	;	54AC	11175	74AC1	1175	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
fmax			90	120		90		90		MHz
<b>+</b> =	CLR	Any Q	2.6	7	8.7	2.6	9.9	2.6	9.3	ns
<sup>t</sup> PLH		Any Q	2.6	7	8.7	2.6	9.9	2.6	9.3	115
<b>+</b>	CLR	Any Q	2.5	10	11.6	2.5	13	2.5	12.4	20
<sup>t</sup> PHL	CLR	Any Q	2.5	10	11.6	2.5	13	2.5	12.4	ns
+	CLK	Any Q	2.4	6.8	8.7	2.4	9.4	2.4	9.1	ns
<sup>t</sup> PLH	CLK	Any Q	2.4	6.8	8.7	2.4	9.4	2.4	9.1	115
<b>+</b> =	CLK	Any Q	1.7	9.4	11.7	1.7	13	1.7	12.5	20
<sup>t</sup> PHL	CLK	Any Q	1.7	9.4	11.7	1.7	13	1.7	12.5	ns

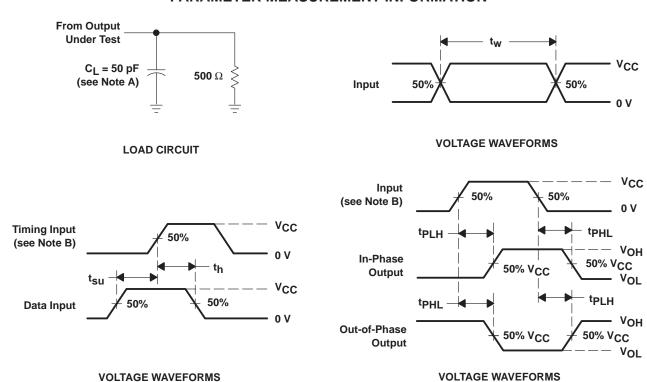
# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	ADAMETED FROM TO		T,	<b>Վ = 25°</b> C	;	54AC1	1175	74AC1	11175	UNIT
FARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	ONIT
f <sub>max</sub>			125	150		125		125		MHz
<b>+</b>	0.15	Any Q	2.2	4.5	6.3	2.2	7.1	2.2	6.8	20
<sup>t</sup> PLH	CLR	Any Q	2.2	4.5	6.3	2.2	7.1	2.2	6.8	6.8 ns
<b></b>		Any Q	2.4	6.7	8.5	2.4	9.7	2.4	9.3	
<sup>t</sup> PHL	CLR	Any Q	2.4	6.7	8.5	2.4	9.7	2.4	9.3	ns
*	CLK	Any Q	2.2	4.5	6.3	2.2	7.2	2.2	6.9	
<sup>t</sup> PLH	CLK	Any Q	2.2	4.5	6.3	2.2	7.2	2.2	6.9	5.9 ns
	Any Q	1.9	6.4	8.5	1.9	9.7	1.9	9.3		
ЧРНL 	t <sub>PHL</sub> CLK	Any Q	1.9	6.4	8.5	1.9	9.7	1.9	9.3	ns

### operating characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	$C_L = 50 \text{ pF}, \qquad f = 1 \text{ MHz}$	48	pF

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \ \Omega$ ,  $t_f = 3 \ ns$ ,  $t_f = 3 \ ns$ .
- $\ensuremath{\text{C}}.$  The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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